**Department of Computer Systems Engineering**

**University of Engineering and Technology, Peshawar**



**DSD Lab**

**LAB #10:**

**NAME: Tiham khan**

**Reg No: 19PWCSE1807**

**Class Section:** A

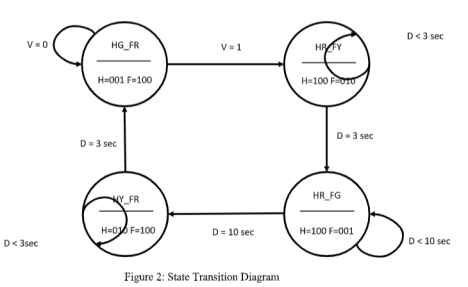
**Submitted to:Engr. Mam Madiha Sher**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

**Traffic Light Controller**

**Task # 09**

Implement Traffic Lighth Controller using FSM.



**Traffic Lights Code:**

| module Traffic\_lights(clk,rst,v,out\_farm,out\_highway);  input clk,rst,v;  output reg [2:0] out\_farm, out\_highway;  reg [1:0] PS,NS;  parameter [1:0] FR\_HG = 0, FY\_HR = 1, FG\_HR = 2, FR\_HY = 3;  parameter [2:0] red = 100, yellow = 010, green = 001;  wire out\_clk;  clk\_divider d1(clk,out\_clk,rst);  always @(posedge out\_clk)  if(rst==0)  begin  PS = FR\_HG;  end  else  PS = NS; |
| --- |

| always @(PS or v or rst)  case(PS)  FR\_HG:  begin  NS = v?FY\_HR: FR\_HG;  out\_highway = v?red:green;  out\_farm = v?yellow:red;  end  FY\_HR:  begin  NS = FG\_HR;  out\_highway = red;  out\_farm = green;  end  FG\_HR:  begin  NS = FR\_HY;  out\_highway = yellow;  out\_farm = red;  end  FR\_HY:  begin  NS = FR\_HG;  out\_highway = green;  out\_farm = red;  end  endcase  endmodule |
| --- |

**Clock Divider Code:**

| module clk\_divider(input in\_clk,output reg out\_clk, input rst);  reg [100:0] count;  always @(posedge in\_clk)  if(rst==0)  begin  out\_clk = 0;  count = 0;  end  else  begin  count = count+1;  if(count==3\*100000000)  begin  out\_clk = ~out\_clk;  count = 0; |
| --- |

| end  end  endmodule |
| --- |

**UCF file:**

| net "rst" LOC =K18 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP; net "v" LOC =F17 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST | PULLUP; net "clk" LOC =V10 | IOSTANDARD = LVCMOS33 | period = 100MHz;  net "out\_highway[0]" LOC = N16 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST; net "out\_highway[1]" LOC = U17 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST; net "out\_highway[2]" LOC = U18 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST; net "out\_farm[0]" LOC = P15 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST;  net "out\_farm[1]" LOC = P16 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST; net "out\_farm[2]" LOC = N15 | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = FAST; |
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